WHAT IS CLAIMED IS:

1. An ESD protection circuit comprising:

a pad;

a first transistor having a first terminal connected to the pad, a second terminal, and a third terminal connected to a ground line; and

a to-be-protected circuit connected to the pad.

2. The ESD protection circuit of claim 1 and further comprising a second transistor having a fourth terminal connected to the second terminal of the first transistor, a fifth terminal, and a sixth terminal connected to the ground line.

3. The ESD protection circuit of claim 2 and further comprising a delay line having an input, and an output connected to the fifth terminal of the second transistor.

4. The ESD protection circuit of claim 3 wherein the input of the delay line is connected to a power supply pad.

5. The ESD protection circuit of claim 4 wherein the delay line has a delay period required for a signal to pass through the delay line, the delay period being greater than a period of an ESD event.

6. The ESD protection circuit of claim 5 and further comprising a first resistive device connected to the second terminal of the first transistor and the ground line.

7. The ESD protection circuit of claim 6 and further comprising a second resistive device connected to the fourth terminal of the second transistor and the ground line.

8. The ESD protection circuit of claim 1 and further comprising:

a first resistive device connected to the second terminal of the first transistor and the ground line; and

a second transistor having a fourth terminal connected to the second terminal of the first transistor, a fifth terminal, and a sixth terminal connected to the ground line.

9. The ESD protection circuit of claim 8 and further comprising a delay line having an input, and an output connected to the fifth terminal of the second transistor.

10. The ESD protection circuit of claim 9 wherein the input of the delay line is connected to a power supply pad.

11. The ESD protection circuit of claim 10 wherein the delay line has a delay period required for a signal to pass through the delay line, the delay period being greater than a period of an ESD event.

12. The ESD protection circuit of claim 2 wherein the first transistor is a bipolar transistor, and the second terminal is a base.

13. The ESD protection circuit of claim 2 wherein the second transistor is a MOS transistor, and the fifth terminal is a gate.

14. The ESD protection circuit of claim 8 wherein the first transistor is a bipolar transistor, and the second terminal is a base.

15. The ESD protection circuit of claim 14 wherein the second transistor is a bipolar transistor, and the fifth terminal is a gate.